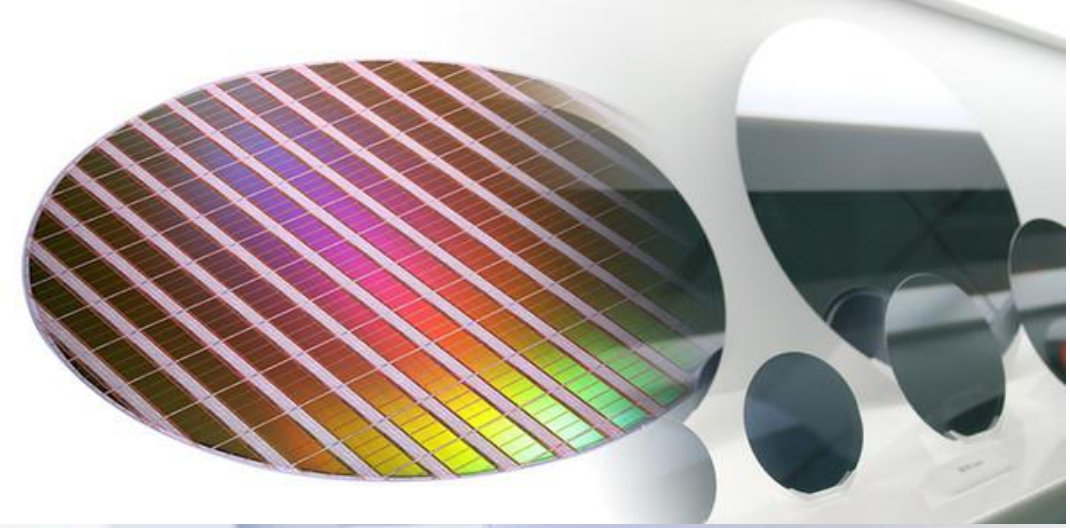

CMPLAB

CMP 실험실

(Chemical Mechanical Planarization Lab)

Department of Mechanical Engineering
Pusan National University

Prof. Haedo Jeong

연도		기관명	직위
1989	1990	한국과학기술연구원	연구원
1990	1991	한국생산기술연구원	연구원
1994	1995	일본 이화학연구소	박사 후 연구원
1995	현재	부산대학교	교수
1999	현재	지앤피테크놀로지(주)	대표이사
2002	2003	UC Berkeley	방문 교수
2002	2004	부산대학교	연구부처장
2004	2013	부산대학교	부속공장장 겸 학교기업 경량부품가공센터장
2004	2013	부산대학교	공과대학 부속공장장
2013	2014	부산대학교	선도기업 인력양성 사업단(LINC) 부단장
2015	2017	부산대학교	선도기업 인력양성 사업단(LINC) 단장

연도		학교명	전공	학위
1980.3	1987.2	부산대학교	생산기계공학	학사
1987.3	1989.2	한국과학기술원	생산공학	석사
1991.10	1994.9	일본동경대학교	정밀공학	박사
논문주제		입자가공에 의한 디바이스의 평탄화에 관한 연구 A study on planarization of device wafer using abrasive processing		

1st Ph.D. for CMP

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Outputs (Career)

Publications

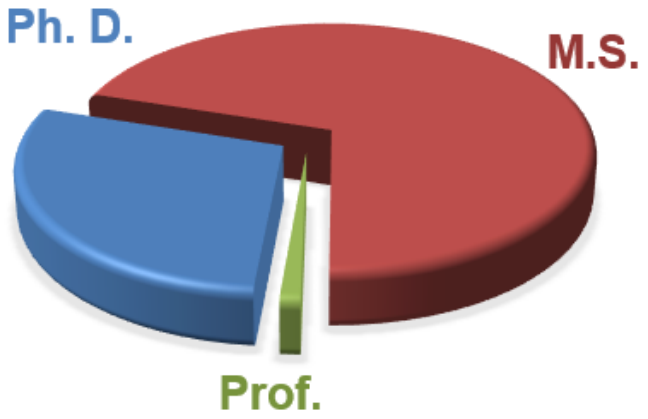
Research papers(370), Conference papers(470), Books(11), Patents(43)

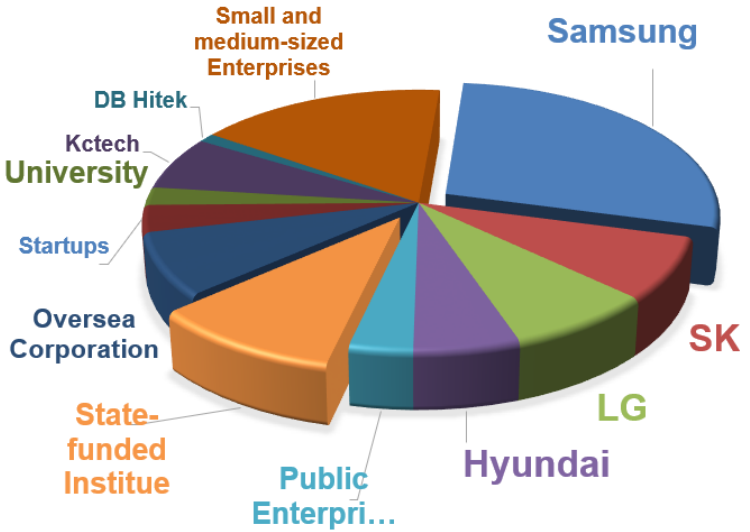
Awards

연도	수상명	수상내용
2018	대통령 포장증	과학기술진흥을 통하여 국가발전에 크게 기여 (과학기술포장)
2017	Most Cited Article Award,2015 to 2016	“Analysis of removal mechanism on oxide CMP using mixed abrasive slurry”
2017	대한기계학회 Outstanding Service Award	Recognition of many years of dedizated service to the mechanical engineering community as an Editor of the Journal of Mechanical Science and Technology
2017	부산대학교 논문상	국내외적으로 저명한 학술지에 다수의 논문을 발표하여 공과대학의 위상을 높이는데 기여
2017	제27회 과학기술우수논문상	“Mechanical Aspects of the Chemical Mechanical Polishing Process:A Review”
2016	키슬러코리아기술상	“Effect of Non-Spherical Colloidal Silica Particles on Removal Rate in Oxide CMP” 등 정밀측정 및 가공분야에서 뛰어난 논문들을 발표하여 정밀공학 발전에 기여
2016	Highly Cited Research	Semi-empirical material removal rate distribution model for SiO2 chemical mechanical polishing(CMP) process
2013	한국정밀공학회 가헌학술상	국내외 학술지 우수 논문 발표 및 정밀 가공 분야 학문 발전에 기여
2012	한국정밀공학회 IJPEM Highly Commended Paper Award	IJPEM Highly Commended Paper Award
2011	부산대학교 우수강의상	우수강의자

Outputs (Alumni)

* Graduates career status: 1998 ~ 2021 (Total 90 people) Ph. D. (26), M.S. (64) Prof. (1)





Members

Ph.D. Student

Seonho Jeong
shjeong@pusan.ac.kr
Research Area
- CMP of advanced package
- Planarization modeling

Master Student

Hoseong Jo
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- Slurry supply system (spray nozzle)

Hogyeong Jo
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- SiC CMP

Minji Kim
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Research Area
- Planarization Modeling

Seongnyeong Heo
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Research Area
- slurry supply system (Ultrasonic waves)

Youngwook Park
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Research Area
-

Yeongil Shin
oil5108@pusan.ac.kr
Research Area
-

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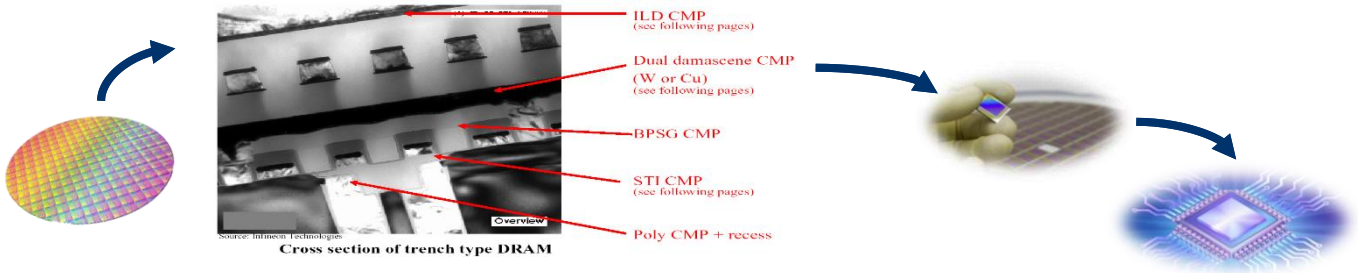
Research contents

차량용 반도체 부족 장기화…국내 업체도 비상

[반도체 슈퍼사이클①]막오른 '반도체 수퍼사이클'…삼성전자, 영업익 50조 돌파 기대

입력 2021-0: 반도체 품귀에 테슬라도 '셧다운'…K반도체 매출 300조 '청신호'

'비수기' 1월 세계 반도체 매출 400억弗 첫 돌파…장기 호황 신호탄



Cross section of trench type DRAM

Increased importance of detailed processes due to increased demand for semiconductor chip !!

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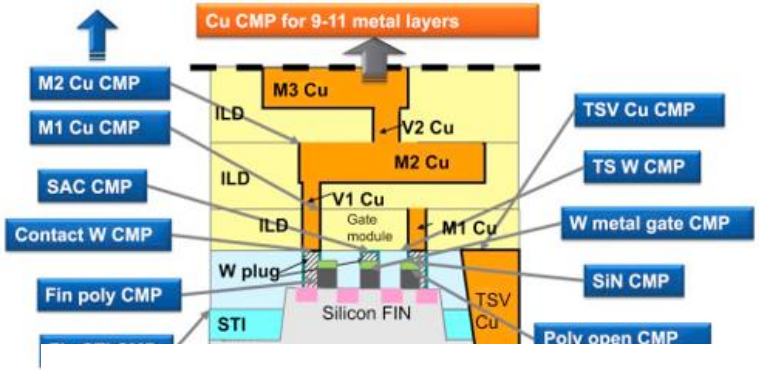
Research contents



The number of CMP processes in advanced semiconductor manufacturing has also expanded up to **20–30 steps**

Memory

Number of CMP Process	DRAM 3Xnm	DRAM 2Xnm	DRAM 1Xnm	NAND 2X - 1Xnm Planar	NAND 3D 32-36L	NAND 3D 48-64L
16						Cu (X)
15						W via (X)
14						W
13			ILD		Cu (X)	W (X)
12		ILD	Cu (X)		W via (X)	W (X)
11		Cu	W via (X)		W	HM (X)
10		W via (X)	TiN		W (X)	ILD4
9	Cu	TiN	ILD4		ILD3	ILD3
8	W via (X)	ILD4	ILD3	Cu	SoP (X)	SoP (X)
7	W	ILD3	W (X)	W (X)	Poly (X)	Poly (X)
6	ILD3	W (X)	ILD2	ILD	SoN (X)	SoN (X)
5	Ox Buff (X)	ILD2	HM Buff (X)	W	HM Buff (X)	HM Buff (X)
4	ILD2	Poly	Poly	ILD	ILD2	ILD2
3	Poly	ILD1	ILD1	Poly	ILD1	ILD1
2	ILD1	Ox Buff	Ox Buff	Ox Buff (X)	Ox Buff (X)	Ox Buff (X)
1	STI	STI	STI	STI	STI	STI
# CMP Layer	10	14	17	10	14-26	17-32
Node Technology	3Xnm	2Xnm DRAM	1Xnm	2X - 1Xnm Planar	3D 32-36L NAND	3D 48-64L

Advanced logic

Number of CMP Process	65nm Planar	45nm HKMG	28nm HKMG	20nm HKMG	16/14/10nm FinFETs	7nm FinFETs	5nm GAA
19							10-11 Cu
18							Co IM (3)
17							HM (4-12)
16						10-13 Cu (*)	W Plugs
15						Co IM (0-2)	W-TS
14						HM (2-6)	Co-TS
13					8-12 Cu (*)	W Plugs	HM
12					HM (2-4)	W-TS	SAC2
11					W-Plugs	SAC2	SAC1
10					W-TS	SAC1	Co Gate
9					SAC	W Gate	HM
8					W-Gate	HM	POP
7				9-10 Cu (*)	HM	POP	ILD0
6			9-10 Cu	W-Plugs	POP	ILD0	Gate Poly
5		7-8 Cu	W	W-TS	ILD0	Gate Poly	III-V
4	7-8 Cu	W	Al / W Gate	Al/W Gate	Gate Poly	SiGe	SiGe
3	W	Al Gate	POP	POP	HM	HM	HM
2	ILD	ILD	ILD	ILD	STI2	STI2	STI2
1	STI	STI	STI	STI	STI1	STI1	STI1
# CMP Layer	10	12	14	15	18-25	24-30	25- 34
Technology Node	65nm Planar	45nm HKMG	28nm HKMG	20nm HKMG	16/14/10nm FinFETs	7nm FinFETs	5nm GAA

(*) Co/TaN barrier in IM

Research contents

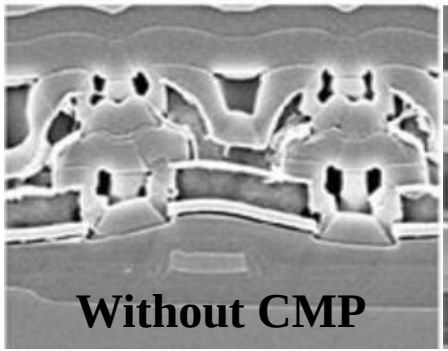
CMP : Chemical Mechanical Planarization

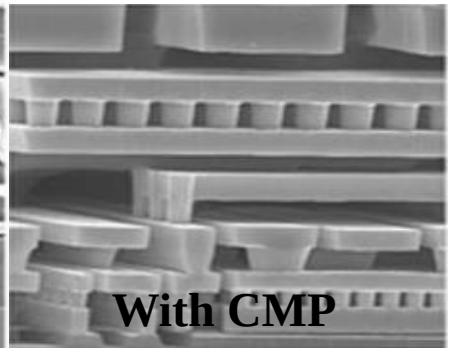
- Polishing unit : 10nm ~ 10Å
- To reduce surface roughness for additional wor

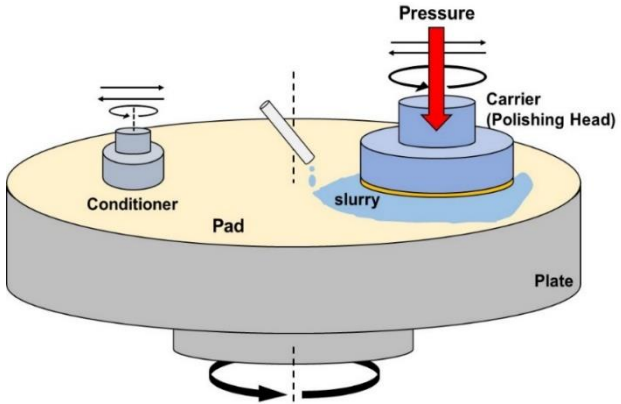
  → Life time ↑ Friction ↓

Technology for …

- Next-generation semiconductor device
- Silicon/compound semiconductor substrates
- Ultra-precise surface processing technology for display/lens
- Micro mechanical/electronic structures using smart materials

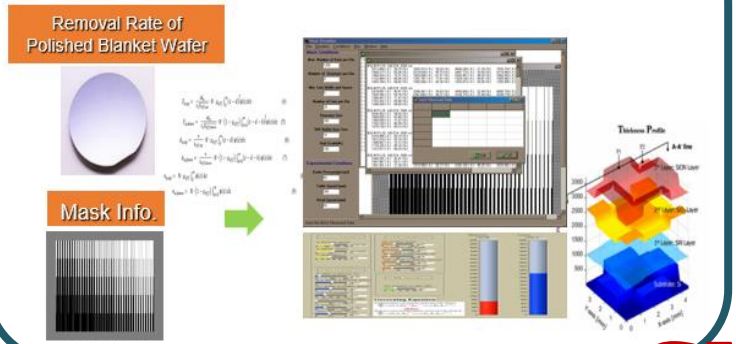




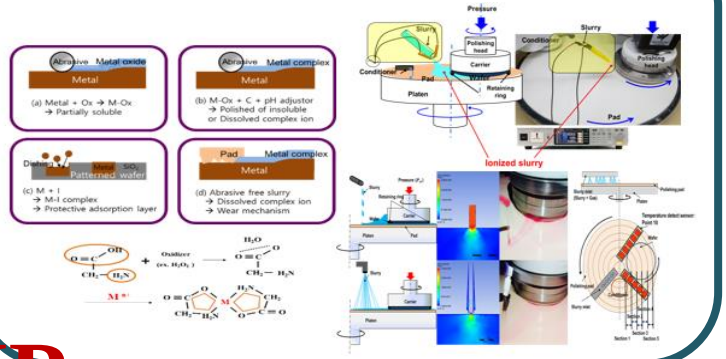


CMP

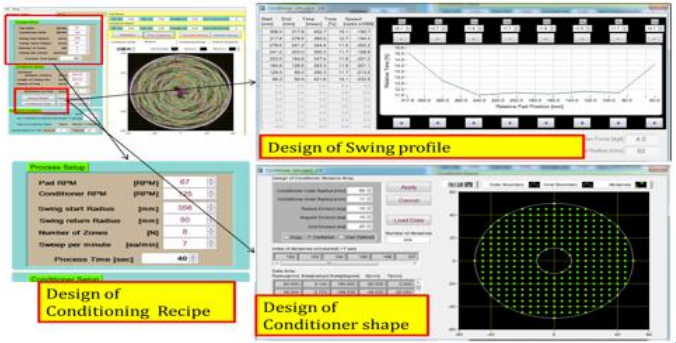
Modeling / Simulation



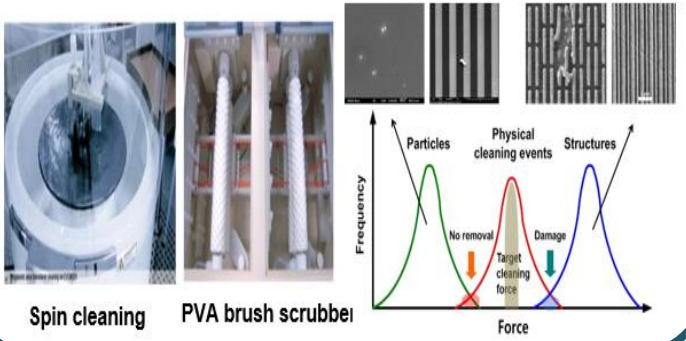
Slurry supply system



Conditioner simulation/ Pad profile



Post CMP cleaning



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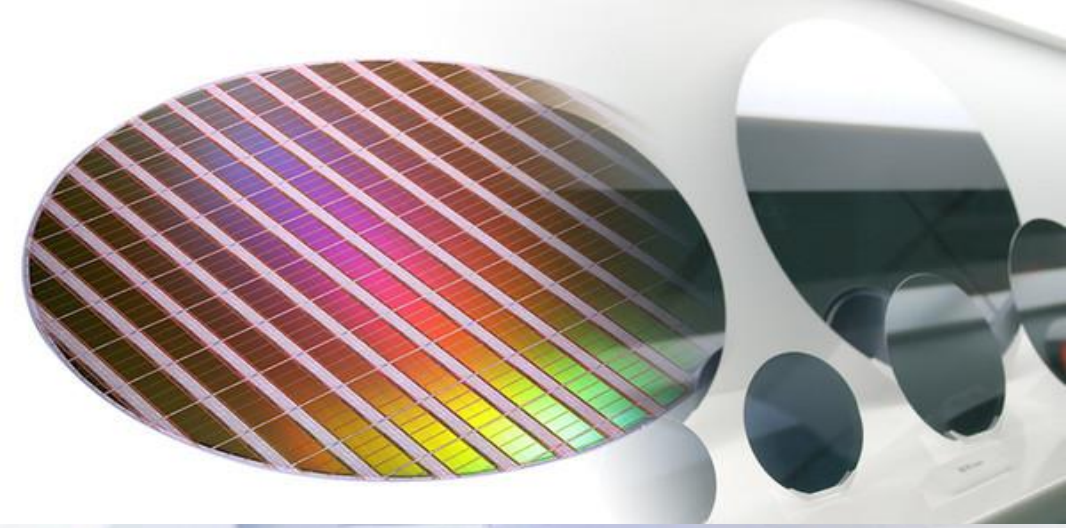

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